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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,856	08/04/2003	Alexander E. Andreev	03-0934/L13.12-0244	5637

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Leo J. Peters
LSI Logic Corporation
1551 McCarthy Boulevard
M/S D-106
Milpitas, CA 95035

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,856	ANDREEV ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 15-20* is/are allowed.

6)☒ Claim(s) *8 and 11-14* is/are rejected.

7)☐ Claim(s) *9-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/633,856 filed on 8/4/2003. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8 and 11-14 are rejected under 35 U.S.C. 103(a) as being obvious over Nanda et al., "A New Methodology for the Design of Asynchronous Digital Circuits," IEEE, 1997, pp. 342-347.

4. As to claim 8, Nanda et al. teach a new logic gate, called the Universal Gate design comprising "AND" and "OR" logic gates. Each of the logic gates has two-rails or nets. A two-input AND gate and OR gate actually has four input lines and two output lines. The inputs basically receive binary "1" and "0", therefore a net is connected to receive the "1" input and a negation net is connected to receive the "0". Similarly, one of the outputs connected to a net to output the "1" and other connected to a negation of the net to output the "0" (see pages 342-345). In order to implement a logic function, the inputs (first, second, third and fourth) are selectively arranged and connected to receive appropriate input states ("1" or "0"). Although, Nanda et al. does not explicitly teach arranging inputs as claimed, it would have been obvious to one of ordinary skill in the art at the time the invention was made to selectively arrange and couple the first,

second, third and fourth inputs to respective first and second nets and negations of the first and second nets, the first and second outputs to a third net and a negation of the third net in order to implement a logic function as desired.

5. As to claim 11, it is well known to practitioner in IC design art that NAND and NOR have been used to substitute AND and OR gates in designing an IC. Therefore, it would have obvious to one of ordinary skill in the art to obtain the relationship as recited in the claim by replacing AND and OR as taught by Nand et al. with NAND and NOR gates to thereby obtain the relationship of equation as recited in the claim.

6. As to claim 12, Nanda et al. teach a first logic gate (AND gate) and a second logic gate (OR gate) in designing a universal gate. Since, NAND and NOR gates are known and can be used in designing an IC, it would have obvious to one of ordinary skill in the art at the time the invention was made to have include NAND and NOR gates in designing the universal gate in order to provide more options to implement IC design to thereby obtain a logic function as desired.

7. As to claim 13, Nanda et al. synthesizing synchronous IC designs using the universal gate (Para. 3).

8. As to claim 14, since inputs lines are connected to receive logic state "0" (negation), it would have obvious to one practitioner in the art that inverter is not needed because this would be cost effective by avoid using additional logic gate.

Allowable Subject Matter

9. Claims 1-7 and 15-20 would be allowable over the prior art of record.

10. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The prior art does not teach or fairly suggest transforming an original netlist to a final netlist by replacing two-input gates and inverters in the original netlist representation by only universal gates, each having four inputs and two outputs, thereby the final netlist representation is obtain to contain only the universal gates.

Remarks

12. Examiner has fully considered the remarks filed on 4/1/2005, but they are not persuasive. Claims 8 and 11-14 are obvious over the teachings of Nanda's article. Nanda teaches an universal gate as claimed (AND or "& "and OR or "+" gates), where each of the AND and OR gate contains four inputs and two outputs as shown in Fig. 2 (top), where two of four inputs connected to two nets (taking logic state "1") and other two of the four inputs connected to the negation of the two nets (taking logic state "0"), and where one of two outputs connected to one net (taking logic state "1") and other connected to the negation of the net (taking logic state "0"). The arrangement of the inputs and outputs to couple to corresponding nets (first, second, third and its negations) are obvious to one of ordinary skill in the art because in order for each of the inputs to receive appropriate logic state "1" or "0", said each of the inputs should be connected an appropriate net that corresponding its logic state "1" or "0", and an output connection should be done in the same manner. For at least these reasons, the claimed limitations are obvious one of practitioner in the art.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER